



128Kx32 3.3V SRAM MULTICHIP PACKAGE PRELIMINARY\*

FEATURES

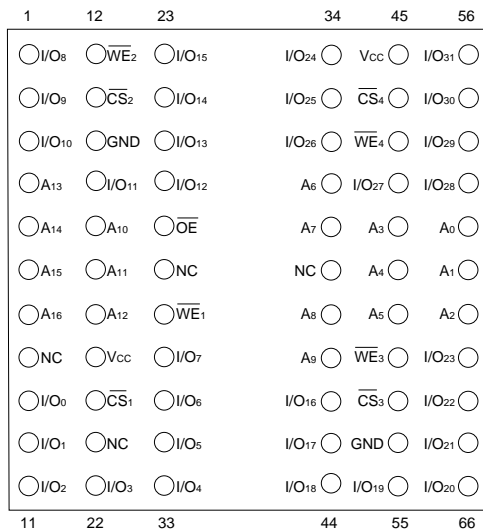
- Access Times of 15\*\*, 17, 20, 25, 35ns
- Low Voltage Operation
- Packaging
  - 66-pin, PGA Type, 1.075 inch square Hermetic Ceramic HIP (Package 400)
  - 68 lead, Hermetic CQFP (G2T), 22.4mm (0.880 inch) square (Package 509), 4.57mm (0.180 inch) high. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 2)
  - 68 lead, Hermetic CQFP (G1U), 23.8mm (0.940 inch) square (Package 509), 3.56mm (0.140 inch) high.
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 3.3 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  - WS128K32V-XG2TX - 8 grams typical
  - WS128K32V-XG1UX - 5 grams typical
  - WS128K32V-XH1X - 13 grams typical

\* This data sheet describes a product that is not fully qualified or characterized and is subject to change without notice.

\*\* Commercial and Industrial temperature ranges only.

FIG. 1 PIN CONFIGURATION FOR WS128K32NV-XH1X

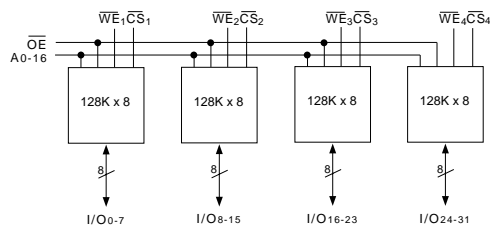
TOP VIEW



PIN DESCRIPTION

I/O <sub>0-31</sub>	Data Inputs/Outputs
A <sub>0-16</sub>	Address Inputs
$\overline{WE}_1-4$	Write Enables
$\overline{CS}_1-4$	Chip Selects
$\overline{OE}$	Output Enable
V <sub>CC</sub>	Power Supply
GND	Ground
NC	Not Connected

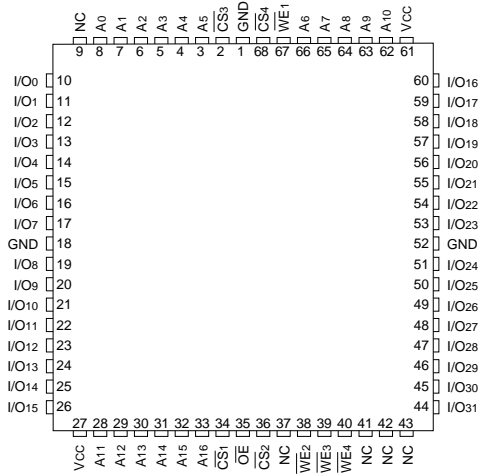
BLOCK DIAGRAM





**FIG. 2 PIN CONFIGURATION FOR WS128K32V-XG2TX AND WS128K32V-XG1UX**

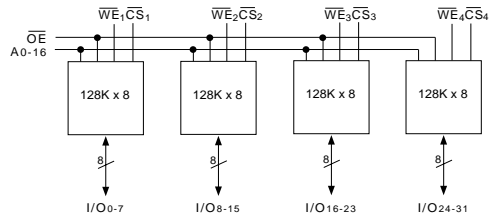
**TOP VIEW**



**PIN DESCRIPTION**

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}1-4$	Write Enables
$\overline{CS}1-4$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

**BLOCK DIAGRAM**





## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.5	4.6	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	5.5	V

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	3.0	3.6	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	+0.8	V

## TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

## CAPACITANCE

(T<sub>A</sub> = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}$ 1-4 capacitance HIP (PGA)	C <sub>WE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	20	pF
CQFP G2T/G1U			20	
$\overline{CS}$ 1-4 capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

## DC CHARACTERISTICS

(V<sub>CC</sub> = 3.3V ±0.3V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Sym	Conditions			Units
			Min	Max	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>CC</sub>		10	μA
Output Leakage Current	I <sub>LO</sub>	$\overline{CS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10	μA
Operating Supply Current (x 32 Mode)	I <sub>CC</sub> x 32	$\overline{CS}$ = V <sub>IL</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz		500	mA
Standby Current	I <sub>SB</sub>	$\overline{CS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz		32	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA	2.4		V



**AC CHARACTERISTICS**  
(V<sub>CC</sub> = 3.3V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	-15*		-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	15		17		20		25		35		ns
Address Access Time	t <sub>AA</sub>		15		17		20		25		35	ns
Output Hold from Address Change	t <sub>OH</sub>	0		0		0		0		0		ns
Chip Select Access Time	t <sub>ACS</sub>		15		17		20		25		35	ns
Output Enable to Output Valid	t <sub>OE</sub>		10		11		12		15		20	ns
Chip Select to Output in Low Z	t <sub>CLZ</sub> <sup>1</sup>	5		5		5		5		5		ns
Output Enable to Output in Low Z	t <sub>OLZ</sub> <sup>1</sup>	5		5		5		5		5		ns
Chip Disable to Output in High Z	t <sub>CHZ</sub> <sup>1</sup>		8		9		10		12		15	ns
Output Disable to Output in High Z	t <sub>OHZ</sub> <sup>1</sup>		8		9		10		12		15	ns

1. This parameter is guaranteed by design but not tested.

\* Commercial and Industrial only.

**AC CHARACTERISTICS**  
(V<sub>CC</sub> = 3.3V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	-15*		-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	15		17		20		25		35		ns
Chip Select to End of Write	t <sub>CW</sub>	13		14		15		20		30		ns
Address Valid to End of Write	t <sub>AW</sub>	13		14		15		20		30		ns
Data Valid to End of Write	t <sub>DW</sub>	10		11		12		15		18		ns
Write Pulse Width	t <sub>WP</sub>	13		14		15		20		30		ns
Address Setup Time	t <sub>AS</sub>	0		0		0		0		0		ns
Address Hold Time	t <sub>AH</sub>	0		0		0		0		0		ns
Output Active from End of Write	t <sub>OW</sub> <sup>1</sup>	5		5		5		5		5		ns
Write Enable to Output in High Z	t <sub>WHZ</sub> <sup>1</sup>		8		9		10		10		15	ns
Data Hold Time	t <sub>DH</sub>	0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

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**FIG. 3**  
**AC TEST CIRCUIT**

The diagram shows a Device Under Test (D.U.T.) connected to a bridge circuit. The bridge consists of four diodes. A current source is connected to the top node of the bridge, with current  $I_{OL}$  flowing out. Another current source is connected to the bottom node, with current  $I_{OH}$  flowing in. The bridge is powered by a bipolar supply  $V_Z \approx 1.5V$ . A capacitor with  $C_{eff} = 50\text{ pf}$  is connected to the D.U.T. input.

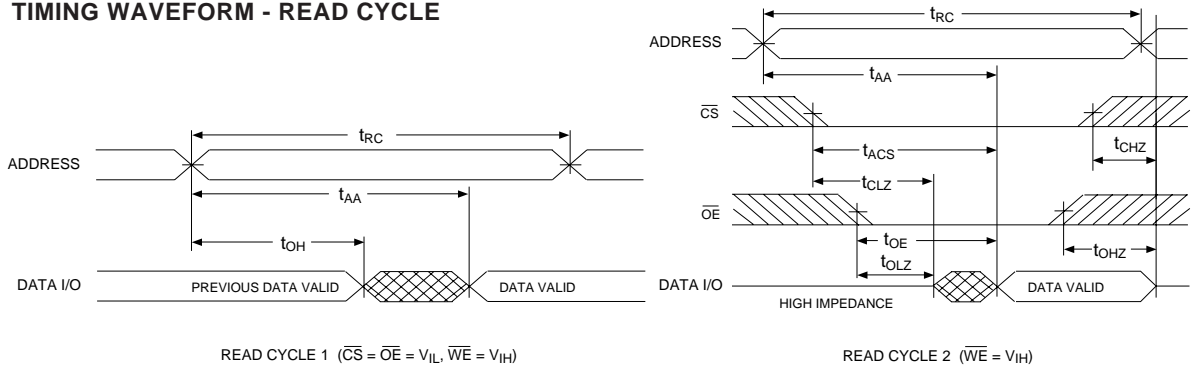
**AC TEST CONDITIONS**

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

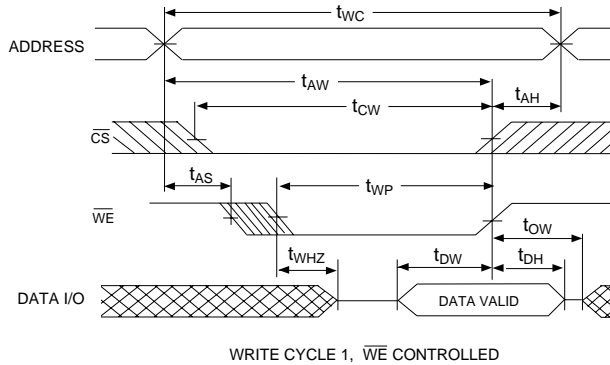
**NOTES:**  
 $V_Z$  is programmable from -2V to +7V.  
 $I_{OL}$  &  $I_{OH}$  programmable from 0 to 16mA.  
Tester Impedance  $Z_0 = 75\ \Omega$ .  
 $V_Z$  is typically the midpoint of  $V_{OH}$  and  $V_{OL}$ .  
 $I_{OL}$  &  $I_{OH}$  are adjusted to simulate a typical resistive load circuit.  
ATE tester includes jig capacitance.



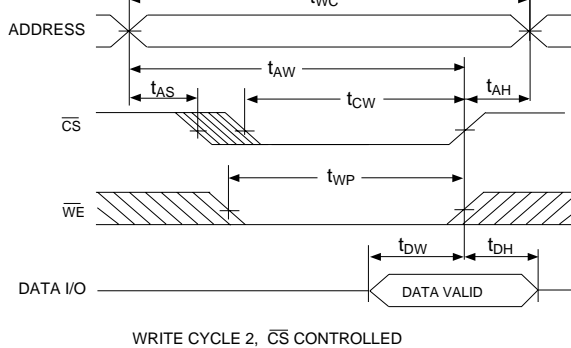
**FIG. 4**  
**TIMING WAVEFORM - READ CYCLE**



**FIG. 5**  
**WRITE CYCLE -  $\overline{WE}$  CONTROLLED**

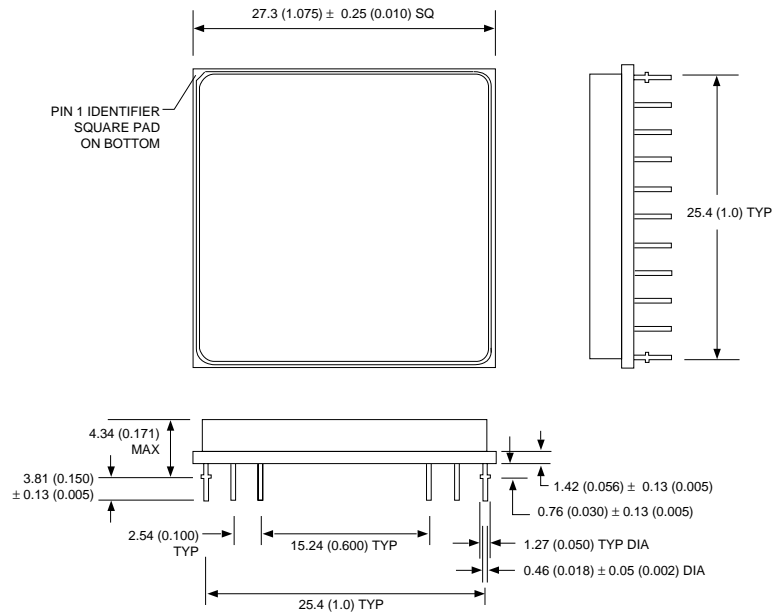


**FIG. 6**  
**WRITE CYCLE -  $\overline{CS}$  CONTROLLED**





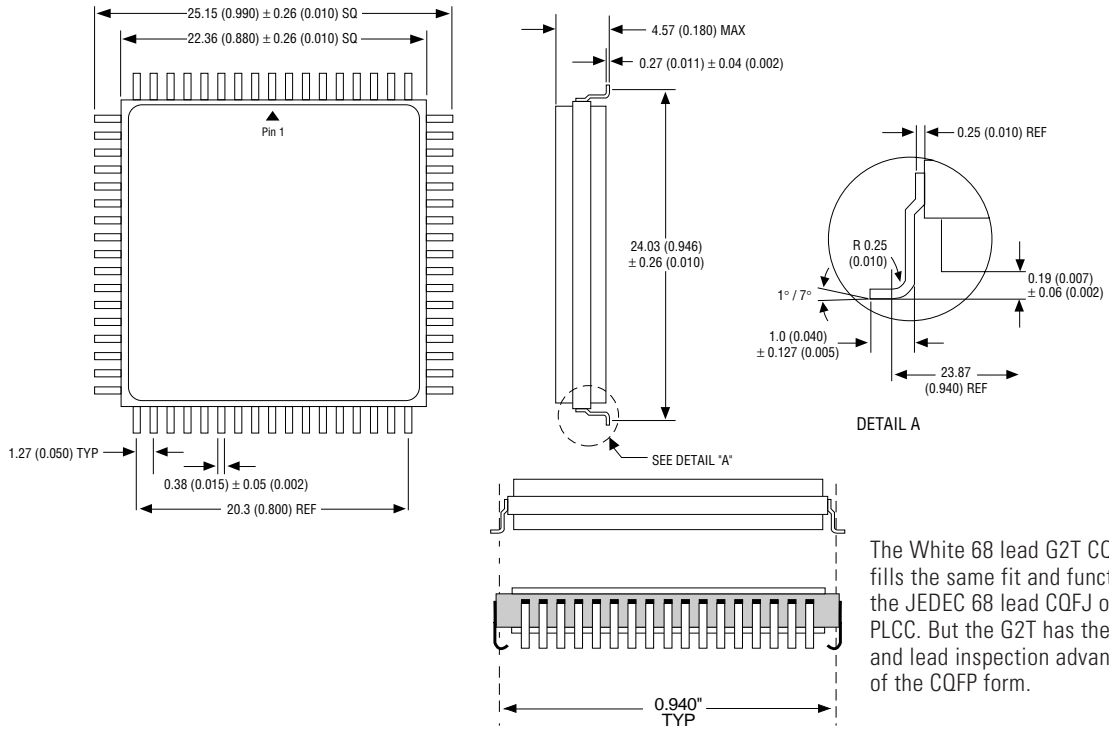
**PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



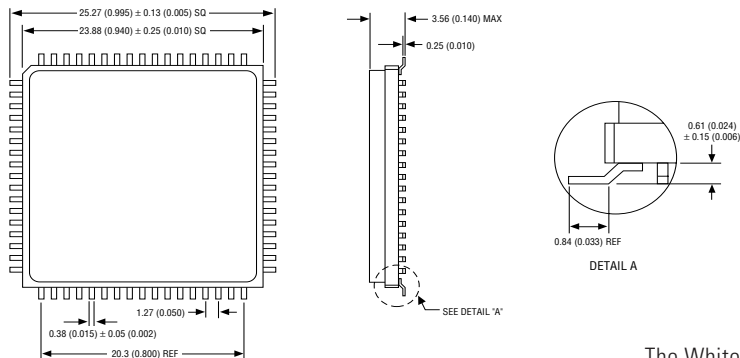
## PACKAGE 509: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)



The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

## PACKAGE 519: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1U)



The White 68 lead G1U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G1U has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



**ORDERING INFORMATION**

**W S 128K 32 X V - XXX X X X**

**LEAD FINISH:**

Blank = Gold plated leads  
A = Solder dip leads

**DEVICE GRADE:**

M = Military Screened -55°C to +125°C  
I = Industrial -40°C to +85°C  
C = Commercial 0°C to +70°C

**PACKAGE TYPE:**

H1 = Ceramic Hex-In-line Package, HIP (Package 400)  
G2T = 22.4mm CQFP (Package 509)  
G1U = 23.8mm Low Profile CQFP (Package 519)

**ACCESS TIME (ns)**

**Low Voltage Supply 3.3V ± 10%**

**IMPROVEMENT MARK:**

N = No Connect at pins 8, 21, 28, 39 in HIP for upgrade.

**ORGANIZATION, 128Kx32**

User configurable as 256Kx16 or 512Kx8

**SRAM**

**WHITE ELECTRONIC DESIGNS CORP.**